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REPORT

Digital line-store standards conversion: a feasiblity study:

No. 1971/44

Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION

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DIGITAL LINE-STORE STANDARDS CONVERSION : A FEASIBILITY STUDY

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Summary

The present analogue line-store converters which convert video signals from the 625/50 standard to the 405/50 standard required for the V.H.F. transmissions have been in service for several years. Some of these converters will reach the end of their service lives before 405-line transmissions are terminated and will need to be replaced. It was considered worthwhile to investigate the feasibility of a new type of converter which processes the signal in digital form; such a converter should not introduce some of the picture defects experienced with present converters and should be more reliable, thus reducing operating costs.

The objectives of the present study were to prove the technical feasibility of digital processing at the rates required for line-store standards conversion and to provide equipment which could afterwards be used for experiments to determine the optimum interpolation aperture.

The results produced by the prototype converter showed that the necessary high-speed digital processing is entirely feasible and economically viable. The output pictures produced were completely free of the type of defect associated with analogue converters.

1. Introduction

Line-store standards converters are used to produce signals on the 405/50 standard for the V.H.F. network transmitters from signals generated and distributed on the 625/50 standard.

Analogue equipment working on principles outlined in 1960[1] has been used by both the BBC and the ITA for several years. In the BBC there are about 28 of these converters in service (including standby equipment), situated at main VHF transmitting stations.

Some of these converters will reach the end of their service lives in the near future and will need to be either refurbished or replaced. In view of the picture defects they introduce (mainly vertical striations, caused by imperfect matching of the many signal channels), and the requirement that reliability should be improved, it was considered worthwhile to investigate the feasibility of a new line-store converter which made use of digital rather than analogue processing.[2]

The storage of signals in digital form was foreseen in a report on a second type of electronic converter[3] which was developed concurrently with that adopted for service use. The idea of carrying out the entire process of conversion digitally was however totally impractical at that time. More recently, such processing has become feasible; moreover, techniques for converting high-quality video signals from analogue into digital form, and vice versa, are now well established.[4]

The main benefit to be obtained from digital processing is an insensitivity to other than large differences in the characteristics of individual circuit elements, with a consequent increase in the overall reliability of the equipment and a reduction in the time spent in initial setting-up and in-service adjustment. Digital converters could also prove to be cheaper than the present analogue converters because of the projected falling costs of digital circuit elements. (Analogue circuits on the other hand will probably involve, at best, a roughly constant cost – slight reductions in component costs being offset by continually rising manufacturing costs.)

The primary object of the present study was to prove the technical feasibility of a digital line-store converter with currently available components. However, it should be pointed out that such components are likely to improve in the near future; this would make a production converter easier and cheaper to design and build.

A second objective was to provide a basic working structure which could afterwards be used for experiments to determine the optimum interpolation aperture and the accuracy with which interpolation must be carried out in order to achieve a satisfactory picture.

2. Fundamentals of line-store standards conversion

2.1. General

Since this project was concerned with a 625- to 405-line converter, all of the figures and descriptions will be confined to that application. There are, however, no fundamental reasons why the philosophy could not be applied to conversion between other line standards.

Two features of the input 625-line waveform have to be changed by the standards converter before the picture is suitable for displaying on a 405-line display. These features are that:

(a) the information contained within the picture is distributed amongst too many lines (625 lines instead of 405 lines)

(b) each line is of too short a duration (64 μs instead of 98·7 μs).

To change the number of lines in the picture, it is necessary to synthesize each new output line from several input lines, by a mixing process known as interpolation. This produces a waveform containing the lines required at the output but still scanned at the input line rate, with a number of blank input line-periods distributed in a complex but predictable manner amongst the wanted lines.

The duration of the output lines must now be altered to suit the output standard by a time-redistributing unit. The time-redistribution process automatically removes the blank lines in the interpolator output and makes the wanted lines occur at the regular intervals corresponding to the output line standard.

Fig. 1 illustrates the two processes of interpolation and time-redistribution. In principle, there is no reason why the two processes should not be carried out in the reverse order, or even simultaneously.[5] The choice of arrangement used in this work was dictated by the requirement to do further experimental work on the two processes separately, interpolation followed by time-redistribution being most suitable for this.

2.2. The interpolation of digital signals

Fig. 2 shows part of an input and an output raster superimposed, the output having been distorted by an insignificant amount to make the two sets of lines parallel. It can be seen that, in general, each output line falls in the space between two input lines; for example, output line 'a' between input lines 'A' and 'B'. A suitably weighted average of the pair of input lines makes an approximation to the information which would have been present on the output line had the original scene been scanned by that output line.

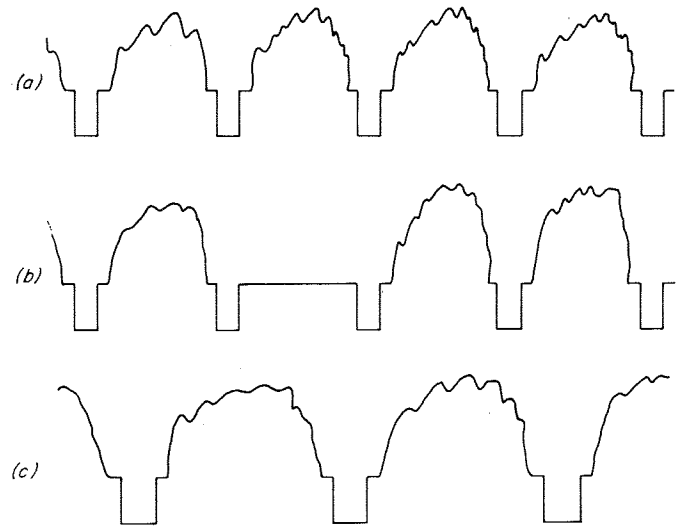

Fig. 1 - Illustration of interpolation followed by time-redistribution

(*a*) 625 input (*b*) Interpolator output (*c*) 405 output

As the lines are time sequential, the input lines used for interpolation must be stored until they are no longer required. In practice, this storage can take the form of tandem delays, each made up of serial shift registers, and each delaying the signal by 1 television line. The number of one-line delays necessary is then one less than the number of input lines needed for interpolation. Fig. 3 is a block schematic of a standards converter, in which a single one-line delay provides two inputs, between which linear mixing can take place in the arithmetic unit.

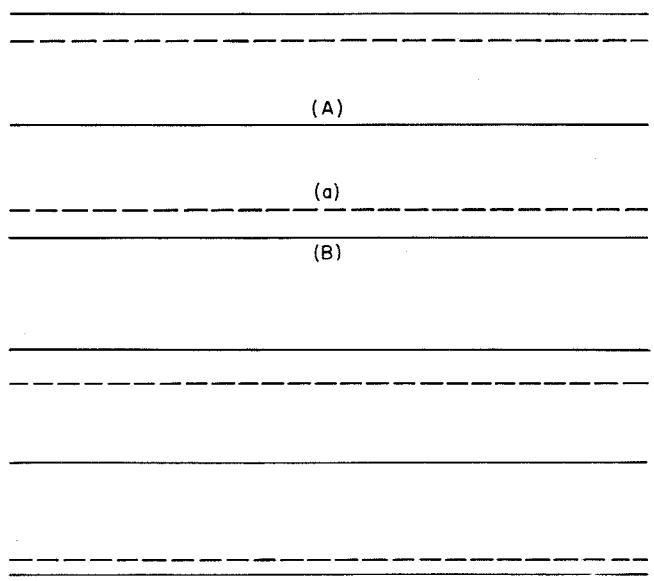

Fig. 2 - Input and Output rasters superimposed

——— input lines — — — output lines

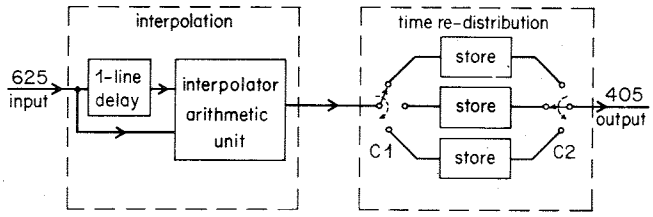

Fig. 3 - Block diagram of digital line-store standards converter

2.3. The time-redistribution of digital signals

Time-redistribution is achieved by the arrangement shown on the right hand side of Fig. 3. Each wanted line, possibly sub-divided into blocks, is written into a digital store or group of stores which is clocked at a rate corresponding to the input standard. The input commutator, C1, steps round one position for each wanted block of data. The information is read out from the stores, via the output commutator, C2, at a rate corresponding to the output standard. The output switch steps round one position for each output data block in the same way that the input switch allowed the information to be written in. After a store has been completely emptied it is available to store another input block. The total number of stores required is, therefore, a function of the maximum length of time for which data must be stored. For conversion from 625 to 405 lines, and a block length of 1 television line, 3 storage units are necessary.

The total amount of storage required can be reduced by shortening the length of the data blocks,[5] at the cost of increasing the complexity of the addressing circuits. The limit is reached when each block is made to contain one picture element; the total storage required for time-redistribution is then slightly more than 1 television line. This arrangement would, however, require a completely uneconomic amount of data-steering circuits, as the inputs and outputs of each of about 600 8-bit word stores would have to be individually accessible.

The experimental converter processed the information in blocks of length 1 line. This led to an economy in design, in that storage units of the same type could be used as delay lines in the interpolator.

2.4. Choice of parameters for the digital signal

The two fundamental parameters of a binary pulse coding system are the sampling or clock frequency and the number of binary digits or bits used to describe the amplitude of each sample.

The number of bits used must be sufficiently large that no visible 'contours' occur when an area of almost uniform brightness is being scanned. The number of bits normally required for broadcast quality television is eight[6] and it was decided to use 8-bit words in the present equipment.

The sampling frequency must be sufficiently high to adequately describe the highest frequency component of the input signal and is normally adjusted to be about two and a half times that highest frequency.[4,7] For 625/50 PAL colour signals the sampling frequency may be either 851 x line frequency when line-locked or 3 x subcarrier frequency if locked to the colour subcarrier; approximately 13·3 MHz in each case.

For 625- to 405-line conversion, the sampling frequency can be reduced because of the relatively restricted upper frequency limit of the 405-line system, equivalent to only 4·63 MHz in the 625-line system. This upper frequency limit is further reduced by the necessity to filter the colour subcarrier and most of its significant sidebands from the input before standards conversion. Fig. 4 shows the spectra of the input and the output signals in terms of a common spatial frequency.

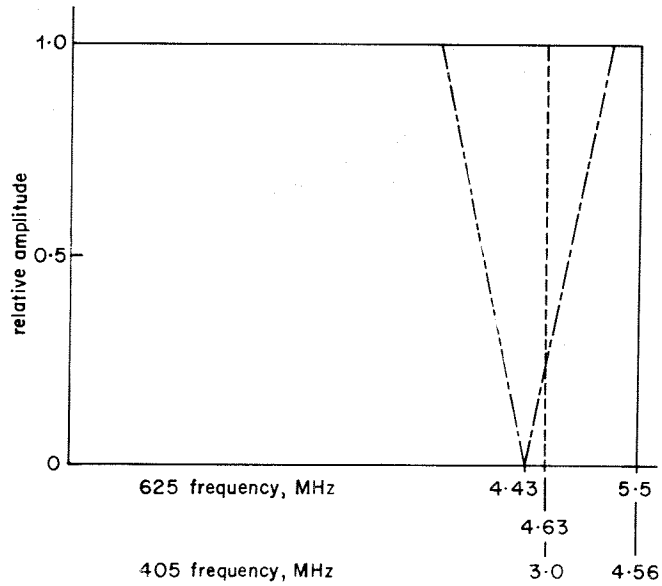

Fig. 4 - 625 and 405 spectra

——— limit of 625 response

– – – – – limit of 405 response

—·—·— colour sub carrier sidebands

A clock frequency of 729 x line frequency, (approximately 11·4 MHz) was therefore chosen for the input signal. This is adequate to describe the highest frequency component of interest in the signal, and leads to convenient numbers for the size of the storage units and to convenient generation of the various clock and trigger pulses required in the converter. At this sampling frequency, a basic storage length of 600 words was sufficient to handle the active line and it will be seen below that this length also suited the type of shift registers used. Appendix I gives an analysis of nominal and full tolerance line timings in terms of clock pulses at 729 x line frequency for both the 625 and 405 waveforms.

3. The storage units

3.1. Operational characteristics

Each storage unit had to have a capacity of about 600 8-bit words with 8-bit parallel access inputs and outputs. It had to be capable of working at clock frequencies of up to

at least 11·4 MHz. Those in the time-redistribution assembly had also to be capable of storing information, when not being clocked, for up to 160 μs.

3.2. Choice of storage elements

A number of different types of digital storage elements were available. These may be divided into three groups.

(1) Magnetic type, including core, thin film and plated wire memories and also disc stores and other similar devices
(2) Bipolar integrated shift registers
(3) M.O.S. integrated shift registers.

Of these, only the M.O.S. integrated shift registers offered a reasonable compromise between speed, cost, package count and reliability (including freedom from maintenance) for the size of store required.

M.O.S. shift registers are themselves divided into two basic types, static and dynamic. In the static type of register, the information is stored in bistable stages and is shifted from one stage to the next by the action of a clock pulse. The information is positively stored between clock pulses, and there is no lower limit on the clock pulse frequency.

In the dynamic type, the information is stored between clock pulses as charge on gate-channel and associated stray capacitances. This capacitance is very small and, together with inevitable leakage currents, has a finite discharge time constant, limiting the storage time and therefore the minimum frequency of operation. The majority of manufacturers guarantee this minimum frequency to be about 1 kHz at 25°C.* However, as the leakage is very temperature dependent (typically 1 decade increase in current for every 44°C temperature rise), the minimum permissible frequency varies rapidly with the temperature of the semiconductor chip. This temperature is a function of the ambient temperature, the average power dissipation on the chip and the thermal resistance to ambient of the package.

When the storage units were designed the majority of devices of this type had a maximum guaranteed clock frequency limit of 2·0 MHz. As the input clock rate was to be about 11·4 MHz each bit channel of the input data had therefore to be sub-divided (or de-multiplexed) into a number of parallel lower-frequency channels. A division factor of 6 was convenient and economic; this permitted the shift registers to operate at very nearly their maximum guaranteed frequency.

As a total capacity of about 600 words was required for each of the storage units, a shift register length of 100 bits, giving the equivalent of 6 x 100 bits of storage (neglecting input and output circuits) was suitable. (The input and output circuits of the storage unit, increased the capacity of each storage unit to 604 words.)

* Semiconductor chip temperature.

The device finally chosen was the General Instruments type DL-6-2100 dual 100-bit dynamic shift register.

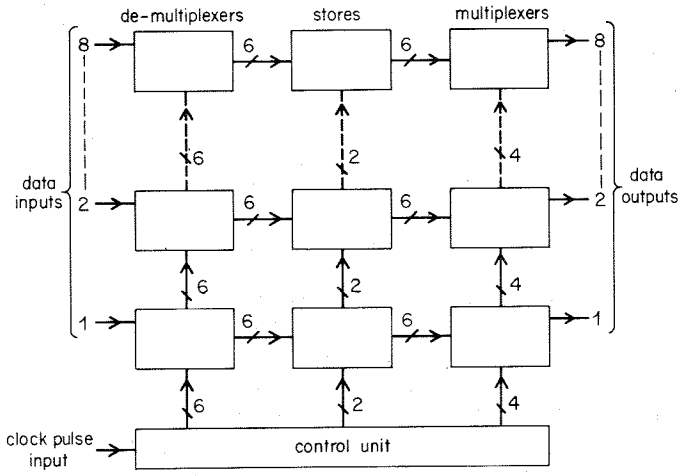

Fig. 5 - Block diagram of storage unit

3.3. Logic design

Fig. 5 shows a block diagram of the one-line storage unit. Each of the eight data channels can be divided into three parts. The first part consists of the de-multiplexing logic which divides the incoming data into six parallel low-frequency channels. The second is the storage assembly, including the T.T.L. to M.O.S. level interfaces at the clock inputs of the shift registers. The third part is the multiplexing logic which re-assembles the data into its original form at the full clock rate. In addition, there is common waveform generating unit which controls the data functions.

To make the unit more versatile and to simplify the interconnections between units, it was decided to subdivide and to re-assemble the data in each unit rather than to process the data throughout the standards converter in 48 parallel, low frequency channels.

3.3.1. Demultiplexing

The part of Fig. 6 labelled 'demultiplexing' shows the arrangement for subdividing the input data. Each bit of the input data stream is presented simultaneously to the inputs of 6 latches. The sample pulse inputs of these latches are driven sequentially by the 6-phase sample waveforms, $P_1 - P_6$. Thus, the output from each latch consists of every sixth bit of the input data, and the six outputs are interleaved in time.

3.3.2. Storage

The arrangement of the storage units is also indicated in Fig. 6. The input to each shift register is compatible with T.T.L. logic levels and is connected to the output of the corresponding demultiplexing latch. Because any input to the set of shift registers is not synchronous with the other inputs of the same set, the shift register clock inputs cannot be driven simultaneously. Ideally, these clock drives should also have six separate phases. In practice, however, the data input set-up times were such

that it was sufficient to divide the set of shift registers into two groups and use two phases of clock drive. As each shift register itself needs two phases of clock drive, these two sets of pulses were obtained simply by interchanging the clock pulse sources ϕ_1 and ϕ_2 so that ϕ_1 for one group of registers becomes ϕ_2 for the other group and vice versa.

As a result of this crossover in the clock drives, it was not possible to use three dual shift registers to obtain the 6 x 100 bits of storage required. Instead, 6 dual shift registers were used to store the data for two channels. The halves of the shift registers not shown in Fig. 6 were used for the other bit channel of the pair.

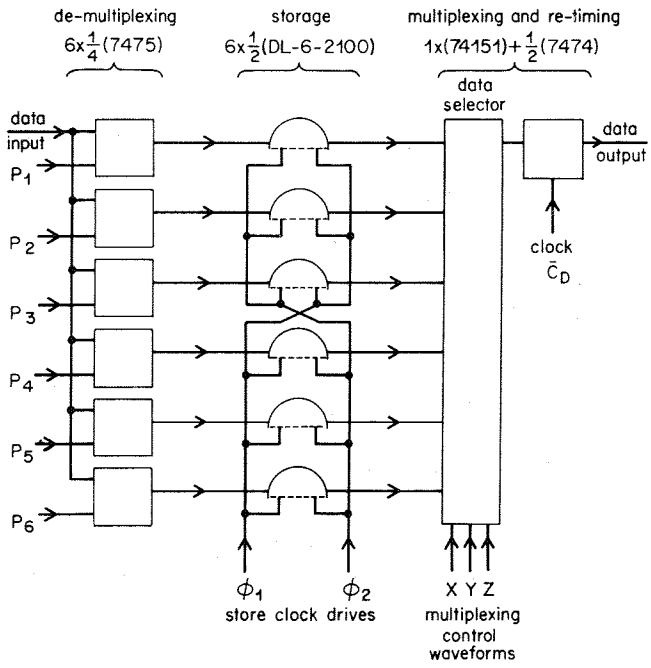

Fig. 6 - Block diagram of 1 channel of storage unit

3.3.3. Data multiplexing

The right hand side of Fig. 6 shows the arrangement used for re-assembling the data carried by the low frequency channels into a single output and re-synchronising the data to a reference clock. The control waveforms 'X', 'Y' and 'Z' were decoded inside the data selectors to give six-phase gating waveforms of the same form as $P_1 - P_6$. Thus the outputs from the shift registers were sampled cyclically in the same order as the inputs were read-in.

In order to allow for the output set-up time of the shift-registers, the input and the output sets of six-phase pulses were arranged to be out of phase with each other.

Finally, the data was clocked out by the reference clock pulses to remove spurious components and to make the output data synchronous with the input data. This gave a standard timing which allows any number of these units to be put in tandem.

3.3.4. Clock drive output stage

The M.O.S. store clock inputs required two phases of drive which were not permitted to overlap. Each of the drive pulses had to have a duration of not less than 200 ns within a total clock period of 526 ns. The total switching time of these two clock waveforms could, therefore, not exceed 526 – (2 x 200) ns, or 126 ns. This means a maximum switching time of approximately 32 ns for each of the four edges.

The load presented to the clock drives by the store was predominantly capacitive totalling 270 pF for 6 clock inputs in parallel. This 270 pF had to be driven through 17 volts in 32 ns. To achieve this slew rate would require a constant current of 145 mA. Because of parasitic inductance it is very difficult to generate a constant current for a significant fraction of 32 ns and in practice the current must have an approximately half-sinusoidal waveform with a peak value of about 300 mA.

Furthermore, since eight clock drive circuits were required for each complete storage unit the individual drivers had to be fairly economic in terms of components.

The circuit shown in Fig. 7 gave a good compromise between performance and component count.

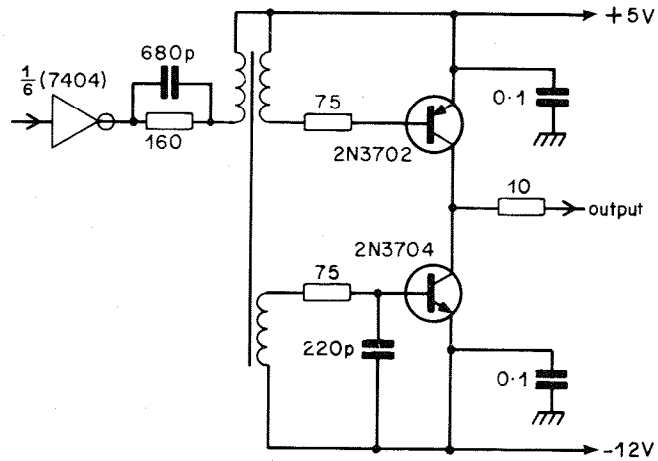

Fig. 7 - Circuit diagram of clock driver stage

3.3.5. Divide-by-six counter and decoder

The control, sampling, and clock waveforms for the different parts of the storage unit were derived from a modulo-six counter which was clocked by the input clock. This is shown in Fig. 8 and consisted of a Johnson ring with protection against the unwanted minor cycle. A number of decoding arrays and buffers were also needed to provide the necessary control pulses with the requisite fan-out capabilities.

3.4. Performance

The complete storage unit, as described above, was constructed on a 10 in. x 10 in. double sided P.C.B.: 24 dual shift registers, 38 dual-in-line T.T.L. packages and 8 discrete clock driver circuits were used in each unit.

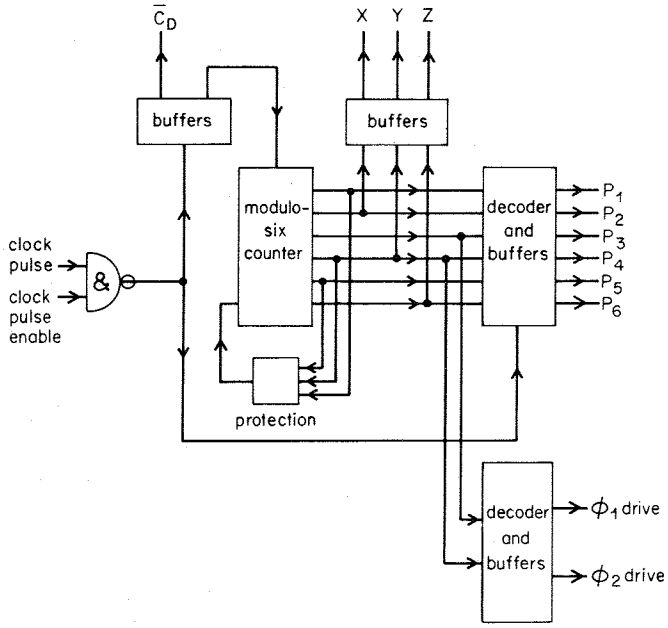

Fig. 8 - Block diagram of divide-by-six counter and control decoding

Of the 96 dual shift registers used, 24 were found to be faulty. Subsequent testing showed that at least one of the two registers in each pack was outside the manufacturers specification. The possibility that these devices had been damaged either before or during the assembly of the storage unit is thought to be unlikely as every precaution was taken to avoid the build-up of static charge. An analysis of the tests carried out on the reject devices did not reveal the sort of catastrophic failure normally associated with mishandling.

In retrospect, it would have been preferable to carry out acceptance tests on each device before assembly, however, it was thought at the time that the increased handling which these testing would entail might itself lead to more failures.

4. Interpolator arithmetic unit

4.1. Function

The interpolator arithmetic unit took in two eight bit words 'A' and 'B', and one three bit interpolation coefficient 'S' and performed the operation:

$$Y = A(1 - S/8) + B.S/8 \text{ (For } S = 0 \rightarrow 7)$$

where Y is the output word, rounded off to eight bits, and represents the 8-level quantised mixing of the two input words. The operation had to be carried out at such a rate that a new output word was available for every clock pulse, that is, an output word rate of approximately 11·4 MHz.

4.2. Design

A complete description of this circuit* is given elsewhere.[8] Basically, the arithmetic unit consisted of a rectangular matrix of data selectors and an array of full adders as shown in Fig. 9. The two inputs to the data selectors were 8-bit parallel words and the operation was controlled by the three-bit interpolation coefficient.

The outputs of the data selectors were connected to the inputs of the array of full adders which summed the data selector outputs. By permanently wiring in a logical '1' at a level immediately below that of the least significant output bit a true rounding-off was obtained.

In order to allow time for the logic to operate, the whole unit was partitioned into time-zones by the insertion of clocked delay stages. Restricting the number of operations carried out during any one clock period in this way permitted operation at the requisite clock rate. In Fig. 9 the clocked stages are represented by the transverse bars. The overall delay of 7 clock periods introduced by this technique was of no consequence.

* The original design was due to J.P. Chambers.

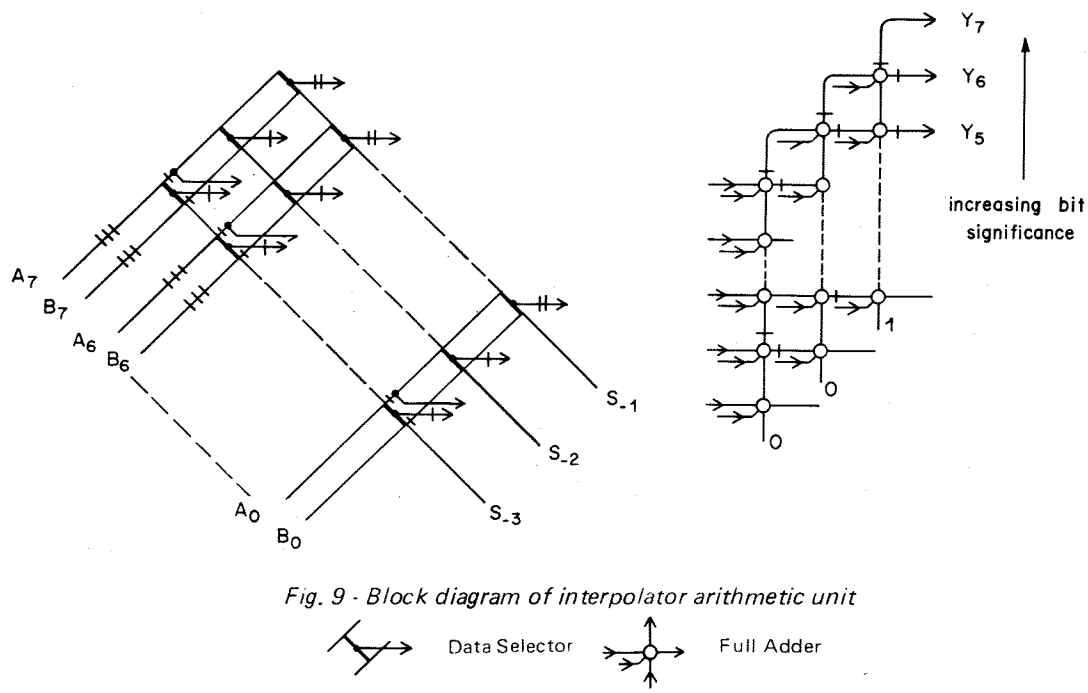

Fig. 9 - Block diagram of interpolator arithmetic unit

As so far described, the arithmetic unit adds the products of one input and the interpolation coefficient to the second input and the binary digits complement of the interpolation coefficient. This gives the function

$$Y = A(7/8 - S/8) + B.S/8 \quad (\text{For } S = 0 \rightarrow 7)$$

To cover the required range of linear interpolation, the factor A/8 was permanently wired in. The range of the output was then limited to between Y = (A/8 + B.7/8) and Y = A.

This slight restriction on the range was not significant in the line interpolation process provided that A was made the direct input and B the delayed input. Under these circumstances the one unobtainable condition

$$Y = B$$

was never required.

5. Control system

The function of the control system was to provide all of the necessary pulse trains for clocking the data, controlling the interpolation and time redistribution processes, and to provide the 405-line synchronising waveform. The system was divided into two areas, firstly, the derivation of the basic pulse and clock waveforms and, secondly, operations on the basic waveforms in order to derive the necessary control waveforms.

5.1. Pulse generation

The basic pulses required were:

625 line trigger	(f_1)
625 clock frequency	($729 \times f_1$)
405 line trigger	(f_2)
405 clock frequency	($729 \times f_2$)
405 mid-line trigger	(f_2')
Lowest common multiple of 625 and 405 line frequencies ($81 \times f_1 = 125 \times f_2 \cong 1{\cdot}27$ MHz) (L.C.M.)	
Field trigger	(F.T.)

Fig. 10 is a block schematic showing the arrangement by which all of these basic pulses were derived from the 625 video input signal.

With the exceptions of the 405 clock pulses, the 625 line trigger and the field trigger, all of the above pulses were derived from the 625 clock frequency by division. This made the pulses mutually synchronous and enabled logical operations to be carried out more easily.

The 625 clock frequency was chosen for this purpose partly because it is a common multiple of the two line frequencies. This made the derivation of the 405 line trigger pulse a matter of simple division, although in practice it was more convenient to use the lowest common

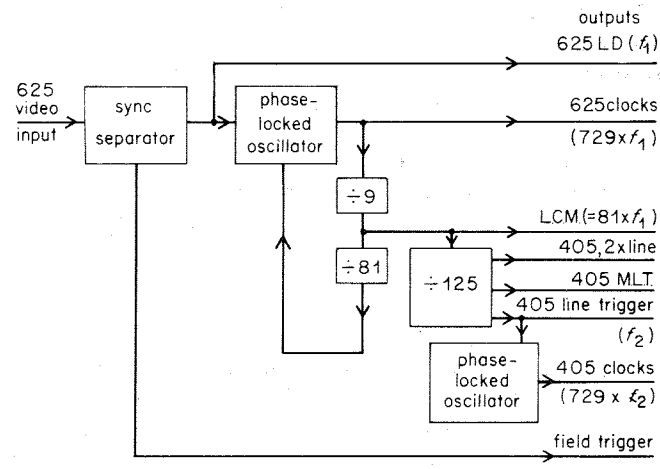

Fig. 10 - Block diagram of pulse generating system

multiple of the line frequencies for most of the logical operations. The 625 clock frequency was therefore divided first by 9 to give the L.C.M. which was then further divided by 125 to give f_2. The 405 clock frequency ($729 \times f_2$) was generated by a second phase locked oscillator, using the 405 line trigger pulses as the reference input.

5.2. Control logic

A block diagram of the control logic is given in Fig. 11.

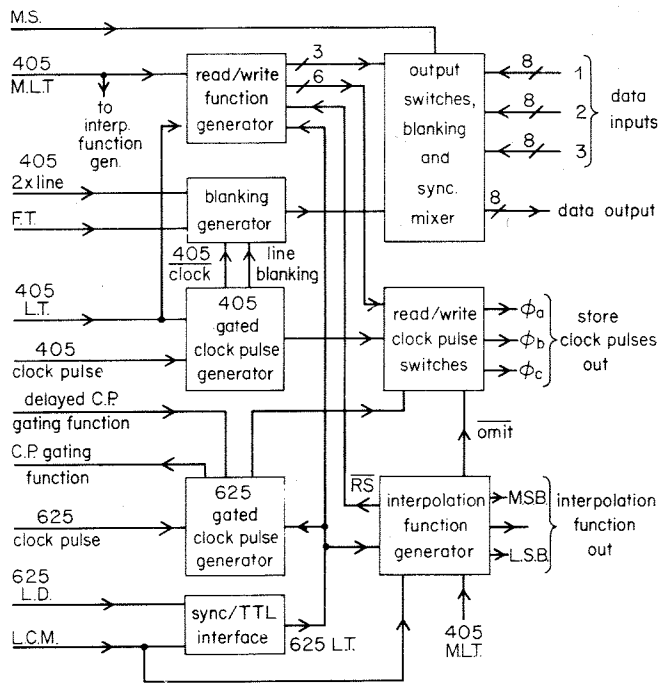

Fig. 11 - Block diagram of control logic

5.2.1. Gated clock generators

The storage units stored only the active part of the television line and the clock pulses used to drive these units had to be gated in such a way that the number of pulses in each block was equal to the capacity of storage unit, that is

604. In addition, the timing of the blocks relative to the synchronising pulses had to be suitably adjusted so as to read in the correct position of the 625 input lines and to give a standard 405-line output (Appendix 1).

The two gated clock generators were similar. Each consisted of a truncated pseudo-random sequence generator shifting at the clock frequency, together with suitable detectors for the states corresponding to the beginning and the end of the block of pulses.

The sequence was started by the edge of the line trigger pulse. The counting continued, with the clock generator output disconnected, until the state corresponding to the beginning of the active line was reached. A bistable circuit was then triggered, enabling the clock output. After a further 604 clock pulses an end-state detector reset the bistable circuit and the sequence generator was returned to its start point ready for the next line trigger pulse.

5.2.2. Interpolation function generator

The function of this unit was to determine the interpolation coefficient from the 405- and 625-line trigger pulses. This operation was based on the fact that a valid interpolation coefficient can be obtained by measuring the position of a 405 line pulse relative to two consecutive 625 line pulses. For convenience, the two sets of pulses used were the 405 and the 625 line trigger pulses. Thus, if the time interval between two consecutive 625 line trigger pulses for line A and for line B is divided into n equal parts and the 405 line pulse occurs after m of these parts ($m \leqslant n$) then a valid linear interpolation coefficient for the output line is obtained by taking:

$$(1 - m/n)\ \mathrm{A} + m/n\ \mathrm{B}$$

In the present case, where the interpolation coefficient had three bit accuracy, $n = 8$.

Fig. 12 shows the basis of the interpolation function generator. This worked by sampling, with the 405 line trigger pulse, a binary-coded octal counter. This counter was synchronised to the 625 line trigger pulse and counted at 8 times 625 line frequency. The sampled output was re-sampled by the 625 line pulse to ensure that changes in interpolation coefficient were made synchronous with the beginning of the new input lines.

Fig. 13 shows how the system provided the correct interpolation coefficient at the time when it is required, that is at the beginning of each line at the output of the interpolator.

Two further waveforms were generated by this circuit, both of which were needed in other sections of the control logic. One of these, 'RS', was an output which went to logical '1' after a 625 line trigger pulse and returned to logical '0' after a 405 line trigger pulse.

By sampling the 'RS' waveform with the 625 line trigger pulse, a logical '1' output was obtained only when

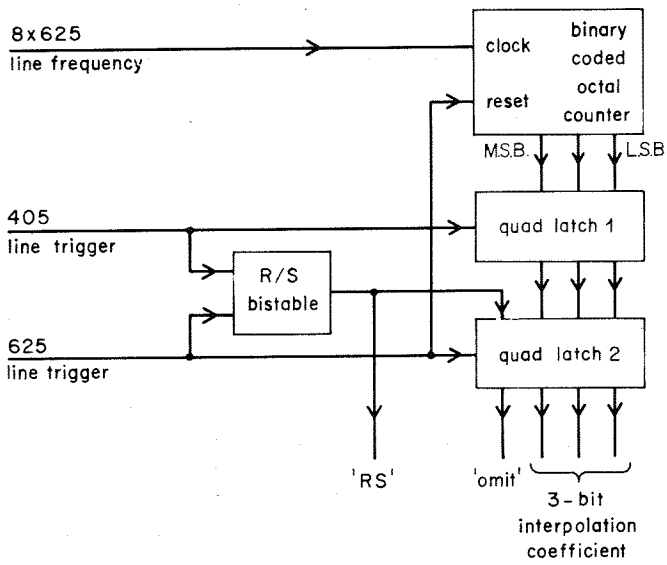

Fig. 12 - Block diagram of interpolating function generator

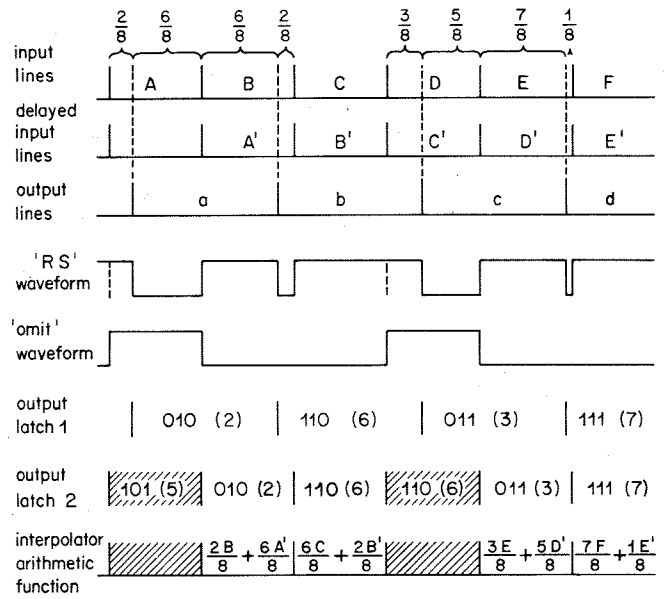

Fig. 13 - Operation of interpolation function generator

there had been no intervening 405 pulse between two consecutive 625 pulses. Reference to Fig. 13 shows that this waveform, labelled 'omit', defines the occurrence of the unwanted output lines from the interpolator.

5.2.3. Read/write function generator

The waveforms controlling the stepping switches, C_1 and C_2 shown in the original block diagram (Fig. 3) were generated by the Read/Write function generator. This unit provided the appropriate control signals for the clock inputs to the storage units.

To prevent reading and writing from occurring simultaneously, it was necessary to phase the two sets of switches correctly. The position of the input switch is uniquely determined by a combination of the output switch position and the state of the 'RS' waveform.

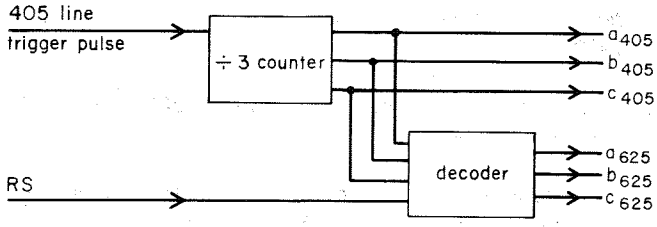

Fig. 14 - Block diagram of read/write function generator

A block diagram of the Read/Write function generator is given in Fig. 14. It consisted of a three state counter advancing one state at the beginning of each output line, thus providing the three sets of read-out control waveforms. Gating circuits, combining the read-out and the 'RS' waveforms, generated the 625 write control waveforms.

5.2.4. Clock switches

Each of the three time-redistribution stores required 405 and 625 gated clocks alternately. The three combined clock waveforms for the stores were obtained from an array of gates whose inputs were the 625 and the 405 gated clocks. These gates were controlled by the 405 read-out the 625 write-in and the 'omit' waveforms.

5.2.5. Read-out and write-in switches

If the outputs of the three time-redistributing stores are selected only when required then the write-in switches S_2 shown in Fig. 3 are redundant; the three store inputs can be paralleled and the spurious information written into each storage unit during the read-out period is overwritten during the true read-in time.

The switches consisted of eight four-input data selectors, controlled by the three read-out control waveforms, and connected to the outputs of the stores. The fourth inputs to the data selectors were used as part of the digital blanking and synchronising pulse mixer which was also incorporated in this stage. The mixer switched the data outputs to binary numbers equivalent to the synchronising pulse or blanking levels when required.

5.2.6. Blanking and synchronising pulse generator

The output line blanking waveform was taken from the control bistable in the 405 gated clock generator. This waveform must, by definition, be the required line blanking waveform since it also controls the 405 gated clocks. The line synchronising pulse was generated by a monostable triggered by the 405 line trigger pulse. The field blanking and synchronising pulse waveforms were obtained from 405 twice line pulse waveforms (generated by gating together 405 line trigger and 405 mid-line trigger) together with a delayed input field pulse. The delay in the field pulse was set to match the average delay of the video signal through the converter.

The mixed blanking and synchronising waveforms generated by adding the above line and field components were used to control the mixer in the output switching stage.

6. Performance

A number of major problems were encountered during the assembly of the standards converter. The most serious of these was the apparent failure of many of the M.O.S. devices to meet their specification, as described in Section 3.4.

A second major problem arose in the design of the storage units. No provision was originally made in the clock driver output stages to hold the clock inputs at the required d.c. level. The leakage currents of these inputs caused the clock level to drift towards earth potential during the period between successive groups of clock pulses. The resulting level was incorrect for the first clock pulse of each new group and an error occurred in the first bit causing a vertical line of errors at the beginning and at the end of the active-line period. This was concealed in the prototype by including pull-up resistors in the clock drivers to ensure that the behaviour was consistent and then increasing the width of the output blanking to include the first and last bits of the store outputs. The additional blanking did not reduce the width of the true active line because the first and last 6 or 7 bits of information were normally standards-converted input blanking.

A further major problem was encountered with the asynchronous 405 clock pulses. Although most of the system ran from one complete set of logically synchronous pulses, it was not feasible to generate the 405 clock pulses as part of this main pulse system. This sometimes gave rise to errors of ±1 clock pulse periods in the output active line timing, with occasional catastrophic errors which occurred when the 405-line trigger pulse and the 405 clocks produced a very short output pulse after being gated together. This very short pulse triggered some stages of the counter in the gated clock generator but not others, thus giving an erroneous output.

A minor modification to remove the catastrophic errors, by synchronising the line trigger edge to the 405 clocks, was successful. A triggered oscillator would probably be a better solution, as the phase of the clocks relative to the line trigger pulse would then be unaffected by any pulse jitter.

Subjectively, apart from the obvious deficiencies caused by the inadequate interpolation aperture, the output picture was very good. This could be attributed to the total absence of the 'vertical stripe' pattern produced by even the best analogue electronic line-standards converter. This performance was achieved with virtually no adjustment, thus showing one of the major advantages of digital systems.

7. Conclusions

This study has proved that the processing of digital data at the rate required for broadcast quality television standards conversion is entirely feasible. It also showed that this type of processing is economically feasible. The additional possible benefits of increased reliability and reduced maintenance are yet to be proved, but the almost

total absence of any preset or adjustable components should contribute greatly to both of these factors.

8. References

1. British Patent No. 928730, 22nd December 1960.

2. CARBREY, R.L. 1960. Video transmission over telephone cable pairs by pulse code modulation. *Proc. I.R.E.*, 1960, **48**, 9, pp. 1546 – 1561.

3. An outline of synchronous standards conversion using a delay-line interpolator. BBC Research Department Report No. T-096, Serial No. 1962/31.

4. Pulse code modulation of video signals : 8-bit coder and decoder. BBC Research Department Report No. 1970/25.

5. British Patent applications numbers 38270/70 and 9292/71 (Cognate).

6. Pulse code modulation of video signals : subjective study of coding parameters. BBC Research Department Report in course of preparation.

7. Line-store standards conversion : the subjective determination of the necessary number of stores. BBC Research Department Report No. T-123, Serial No. 1964/13.

8. A fast digital linear interpolator. Provisional title of BBC Research Department Report in course of preparation.

9. Appendix

9.1. Line timings

(i) 625 — line standard

All timings are relative to line time reference point.

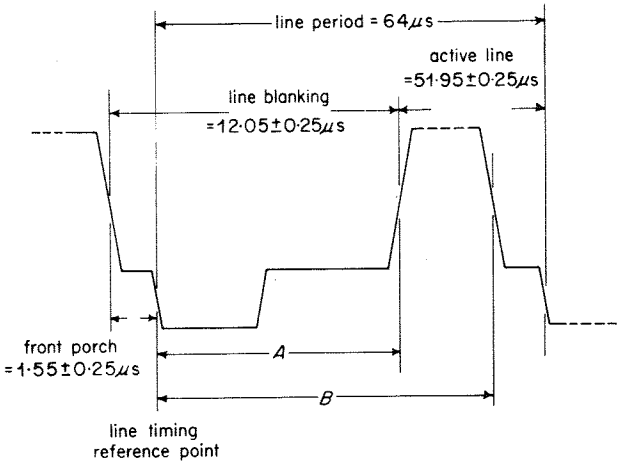

Fig. 15 - 625 line timings

Timings in clock pulse are at 729 x line frequency.

Earliest start of active line	= (12·05 — 0·25) — (1·55 + 0·25) μs
	= 10·0 μs
	= 113·9 clock pulses
Latest start of active line	= (12·05 + 0·25) — (1·55 — 0·25) μs
	= 11·0 μs
	= 125·3 clock pulses
Longest active line	= 52·2 μs
	= 594·6 clock pulses
Latest finish of active line	= 64 — (1·55 — 0·25)
	= 62·7 μs
	= 714·2 clock pulses
Nominal start of active line, *A*	= 10·5 μs
	= 119·6 clock pulses
Nominal end of active line, *B*	= 62·45 μs
	= 711·3 clock pulses
Number of clock pulses in nominal active line	= 591·7

If the gated clock pulse generator gives an output clock pulse for the 114th input pulse after the line trigger and for all subsequent input pulses, up to and including the 717th, that is a total of 604, then:

a) the nominal active line will begin approximately 6 clock pulses after the beginning of the stored line and end approximately 6 clock pulses before the end of the stored line.

b) any active line which begins at the earliest specified time will lose a maximum of 1 sample from the beginning of the line.

c) any line timing later than that in 'b' above will not result in information being omitted.

(ii) 405 — line standard

All timings are relative to the line time reference point.

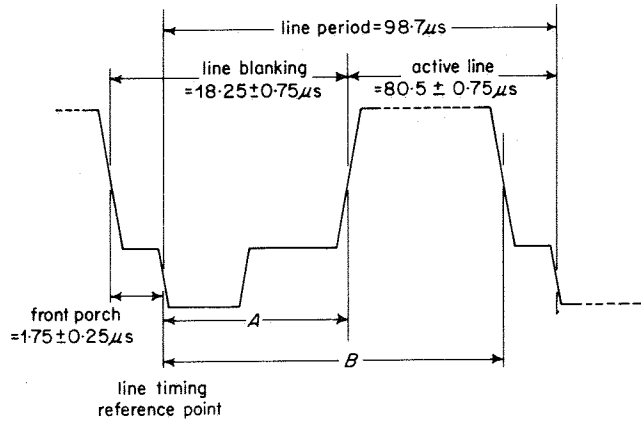

Fig. 16 - 405 line timings

Timings in clock pulses are at 729 x line frequency.

Earliest start of active line	= (18·25 — 0·75) — (1·75 + 0·25)
	= 15·5 μs
	= 114·4 clock pulses
Latest start of active line	= (18·25 + 0·75) — (1·75 — 0·25)
	= 17·5 μs
	= 129·2 clock pulses
Longest active line	= 81·27 μs
	= 599·9 clock pulses
The latest finish of active line	= 98·76 — (1·75 — 0·25)
	= 97·26 μs
	= 717·8 clock pulses
Nominal start of active line, *A*	= 16·5 μs
	= 121·8 clock pulses
Nominal active line length	= 80·55 μs
	= 594·6 clock pulses

If the gated clock generator output starts at the 116th input clock pulse after the line trigger pulse, and continues up to the 720th then:

a) with a nominal input line, with 6 samples of input blanking preceding the active line, the output active

line will begin at pulse number 122 and finish at pulse number 714.

b) with an early input line timing, the output active line may start at pulse number 116.

c) with a late input line timing, the stored line will contain a minimum of 4 samples of blanking after the active line (that is, 718 – 714·2). The output active line will therefore finish at pulse number 716.

All of these timings are within the tolerances given above for the timings of the 405 line waveform.

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